Study of Quantum Cellular Automata Faults

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Abstract -The Quantum cellular automata is a new emerging technology with a high potential in digital circuit implementation, which is faster and more power efficient than the existing conventional MOS technology. The QCA implementation has a advantage of high fault tolerance which gives QCA implementation to use displaced cells in its circuit without losing the functionality. Here we are trying to study various outputs from a QCA array when the cells at different stages are given offset with respect to others. The results are explained with respect to output obtained from QCA Designer provided by University of British Columbia.
Keywords – QCA, Binary wire, tolerance.

INTRODUCTION

Quantum cellular automata is an emerging technology which has the potential of replacing the conventional technology of MOS transistors for implementing digital devices. Various papers have been published on implementing logic gates with QCA. There is also focus on the one of the advantage of QCA that is the cell displacement of a single QCA cell with respect to other cell will not alter the finale output.

In this paper we will be focusing on the variation of the output voltage when the QCA cells are displaced with respect to other cells in different circuits. We will also try to explain some basic concept like quantum cell and binary wire. Most of the simulation is done with respect to a binary wire for calculating the variations in output signal.

I QCA Cell.

A) Cell

The basic quantum cell representation has five quantum dots on the cell, four on the corner and one in the center.

There are two electrons which are free to move across the quantum dots. The electrons automatically orient itself opposite to each other diagonally (antipodal outer sites) in the cell which corresponds to high stability.
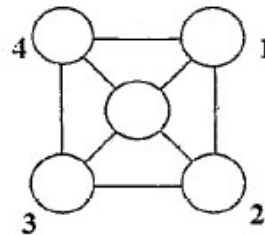

Fig 1. Schematics of a basic five- site cell with 'X' orientation is shown.
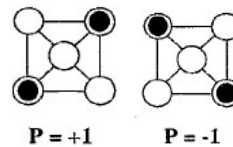

Fig 2 electrons occupying antipodal sites in a cell, this type of orientation is the most stable form. This bistable states is denoted by '+1' and '-1'.

B) Binary wire

Different from conventional ways of transmitting the signal through the circuits in a QCA circuit the cell itself can be used for transmission. The polarization of each cell in quantum cellular automata tends to orient itself the orientation of its neighbor. The binary values '1' and '0' valued as '1' and '-1' in QCA can be transmitted along an array of cells rather than using a wire connection.

The binary wire has an added advantage that it can transmit even when there is some misalignment for the cells. Variation in the output due to cell offset will be discussed further in this paper.

Fig 3 The polarization of the driver cell (input) is transmitted towards the output.

C) Majority Gate

Majority gate is one of the basic gates in QCA which can be programmed to form other digital basic gates such as AND and OR. The majority gate function is given by Maj(ABC) = AB + BC + CA. Implementation of a majority gate is done by 5 QCA cells.

Programming majority gate is done by permanently setting one of the 5 cells into either '1' or '0' for OR and AND respectively.
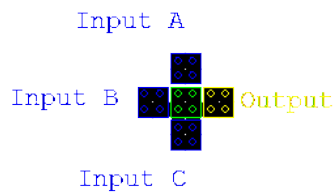

Fig 4. Majority gate implemented using QCA Designer. The inputs "votes" on the polarization of the central cell and the winning polarization is outputted.

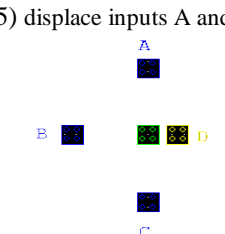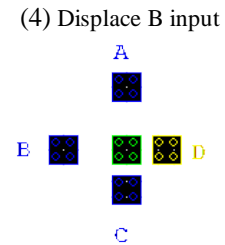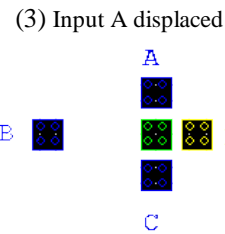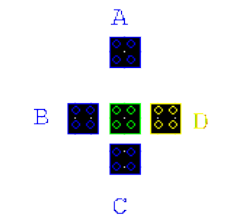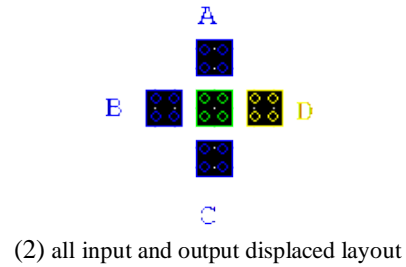## DEFECTS AND TOLERANCE ANALYSIS

I Majority gate

Consider a conventional 5 cell QCA majority gate. Different defects in circuit consist of simple displacement of cells and misalignment.

Displacement fault

Here we have considered various displacement configurations of the cells. The cells are moved with respect to the center cell and output is obtained and compared.
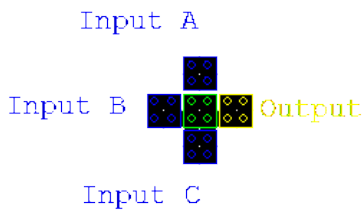
(1) Ordinary majority gate layout

(2) all input and output displaced layout

(3) Input A displaced

(4) Displace B input

(5) displace inputs A and B

(6) Displace all inputs

Fig 5. Displacements in majority voter

We can infer from the simulations of the above layout that the directly opposite input cell (cell B) is dominating with respect to other input cell. This cell has bigger impact on the center cell.

A) Without any displacement

The majority gate gives an output of 9.65eV and all its output have equal amplitude and logic function is given by Maj (ABC) = AB + BC + AC. The configuration is shown in Fig 5 (1).

B) All input and output displaced layout

When the displacement is ≥ 7nm output function is equal to input B. That is D = B.

C) Input A or C displaced

The output follows the majority function till the displacement is ≤ 10nm with no variation in output signal for various input combinations. When the displacement is between 10nm and 20nm the output start to change; showing a dominate effect of input B on the output. Above 20nm the output follows input B.

D) Input B displaced

When input B is displaced the output from majority gates follows the acceptable function upto 20nm without any change in output for different combinations. Above 20nm the signal strength reduces till 45nm. Above 45nm the gate now displays a new function given by Maj(ACB) where B = 0. In this scenario the gate gives an output 'U' where there is no majority.

Table 1 truth table for displacement of B.

Input A	Input B	Input C	Output	Output without displacement
0	0	0	0	0
0	0	1	U	0
0	1	0	0	0
0	1	1	U	1
1	0	0	U	0
1	0	1	1	1
1	1	0	U	1
1	1	1	1	1

E) Input A and B displaced

Output = Maj(ACB) when displacement ≤ 20. Above 20nm the output follows input 'C'.

F) All inputs are displaced

This configuration proves the dominance of input B. Displacement ≤ 20nm will give output same as case in displacement of A or C. The signal gradually decreases but the functionality remains the same. When the displacement becomes larger than 44nm the input B dominates and the output follows a

function which gives the output only when input B has a role in determining the majority.

Table 2 truth table for majority gate with all inputs displaced

Input A	Input B	Input C	Output	Output without displacement
0	0	0	0	0
0	0	1	0	0
0	1	0	U	0
0	1	1	U	1
1	0	0	U	0
1	0	1	U	1
1	1	0	1	1
1	1	1	1	1

Offset fault

Another type of fault that can occur for a QCA circuit is the misalignment fault or offset fault. In this case the cell is out of alignment with rest of the cells in the circuit. The variation of output depends both on the displacement to which the cell is misaligned and also on the direction (to input or output side).

(1) A left offset (2) A right offset (3) AC left offset

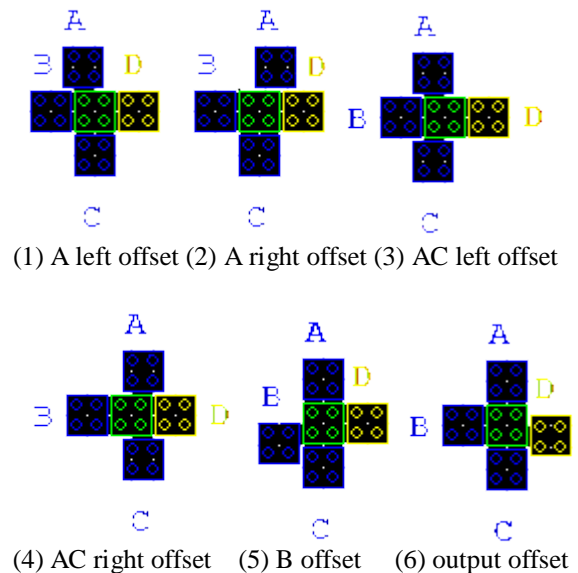(4) AC right offset   (5) B offset   (6) output offset

Fig 6. Offset configurations for majority gate.

Table 3. Maximum offset for which no change in functionality occurs and corresponding direction is given below.

Offset Cell	Direction (left/input side, right/output side)	Max displacement without change in functionality
A or C	Left	≤ 5nm
A or C	Right	≤ 4nm
A and C	Left	≤ 4nm
A and C	Right	≤ 3nm
B	Up or Down	≤ 8nm
D (output)	Up or Down	≤ 4nm

II Binary wire

Binary wire is an major advantage of QCA technology from the conventional MOS technology. The property of QCA cell to align itself with respect to its neighbor's polarization allows us to transmit binary values '1' or '0' (+1 and -1 with respect to QCA) through array of cells avoiding additional interconnection methods.

This has another added advantage that is even when one of the cells is weakly polarized it can still transmit a 'good 1' through the binary wire.

A simple binary wire is being studied here, where cells at various positions are given offsets and output is checked for variations.

(1) Input offset

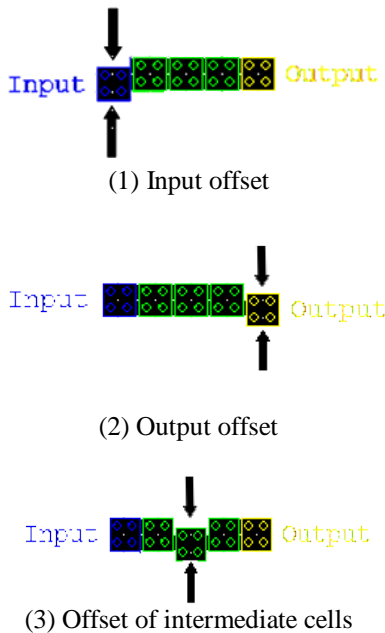(2) Output offset

(3) Offset of intermediate cells

Fig 6. Various offset layout for a binary wire with 5 QCA cell.

The simulation was done with a 5 cell QCA binary wire. The output for the above layouts shows that the more distance the offset cell has from the output the less effect it has on the output.

A) Input offset

The signal level remained the same for a range of 0nm to 25nm offset. The signal got inverted at an offset of 9nm.
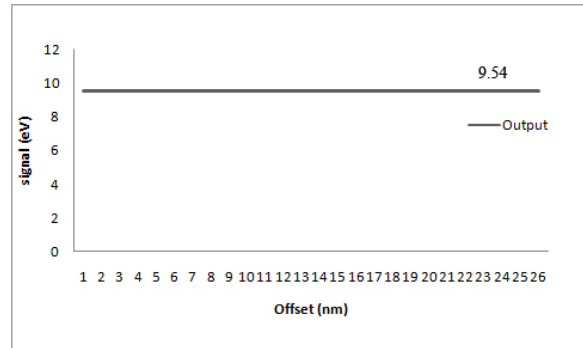

Fig 7 The graph gives the variation in the signal with respect to the offset distance. Samples from 0nm to 25nm are taken for the study. The output was constant 9.54eV.

B) Output offset

There is a large variation in signal when the output cell is at offset. The output was varying from 9.54eV to 3.22eV.
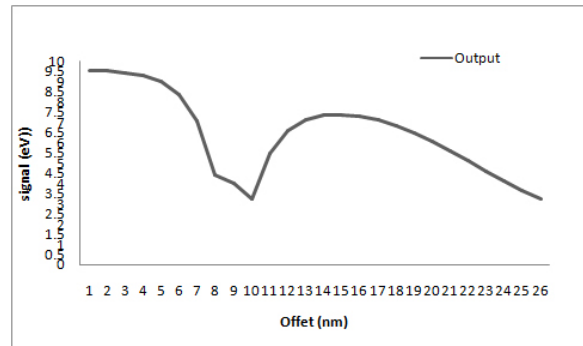

Fig 8 Variation in output is mostly effected by offset in output sell. The figure shows two peaks one for normal transmission where input is transmitted to output and other is the inverted output.

C) Offset for intermediate cells

The effect of offset at intermediate cell declines proportionally with the distance of the cell from the output. The more distance between the cell and the output the less impact it has on the output.
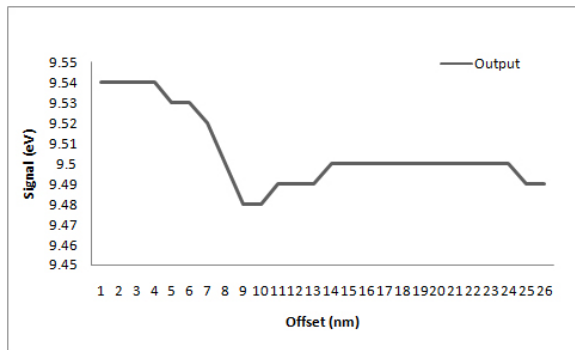
Fig 9 The graph gives the variation of output when the 3rd cell of 5 cell binary wire is displaced (as shown in Fig 6(3)). From the layout it can be assumed that the signal gets inverted twice when the offset is between 15nm and 25nm, which may be the reason the signal is steady at 9.5eV.

CONCLUSION

For majority gate configuration as well as binary wire; faults of ±5nm is permissible, which will only have a minimum degradation of output signal. The effect of offset for any cells on a binary wire reduces with the distance of cell from the output.

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